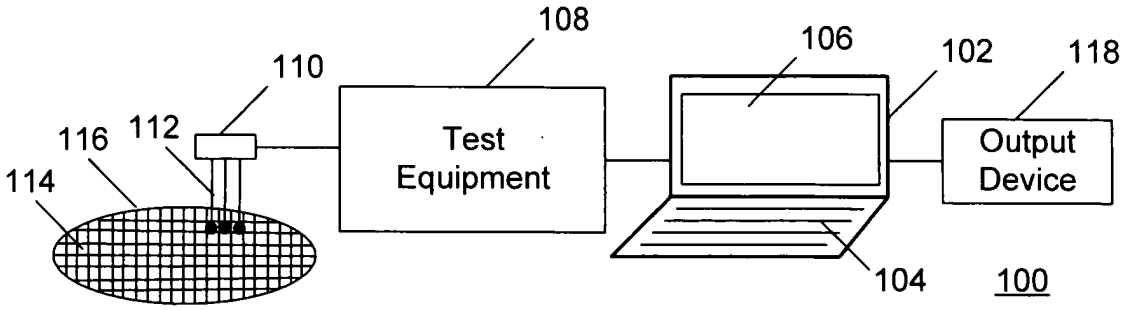

FIG. 1

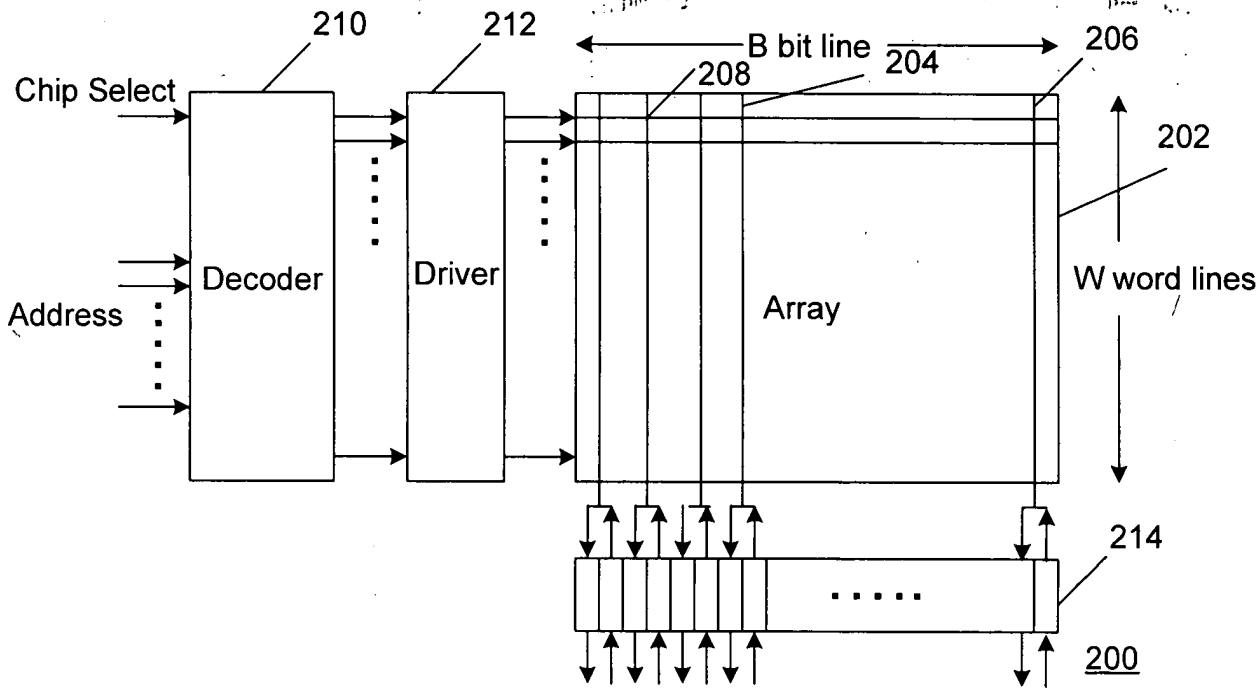

FIG. 2

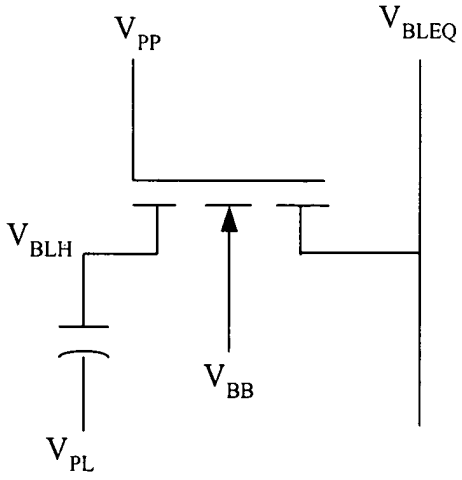

FIG. 3

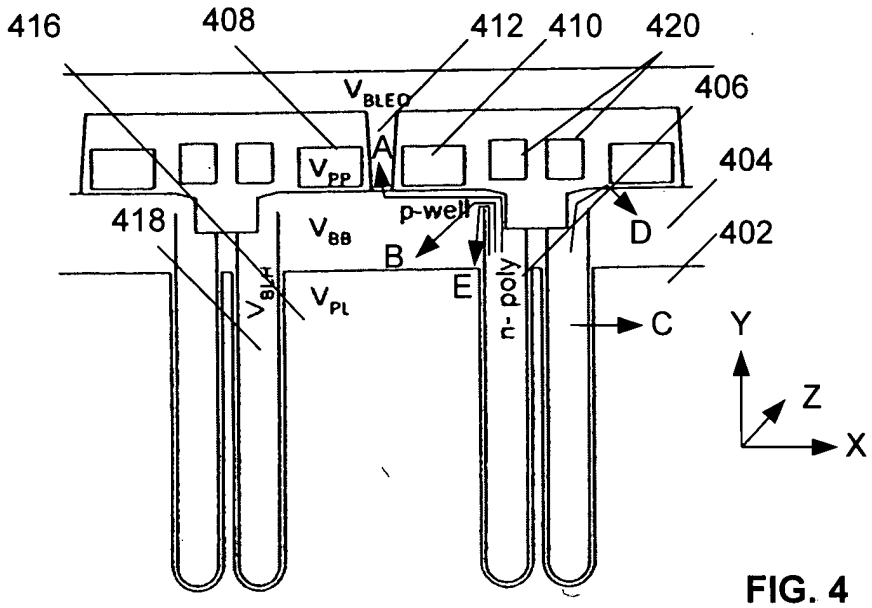

FIG. 4

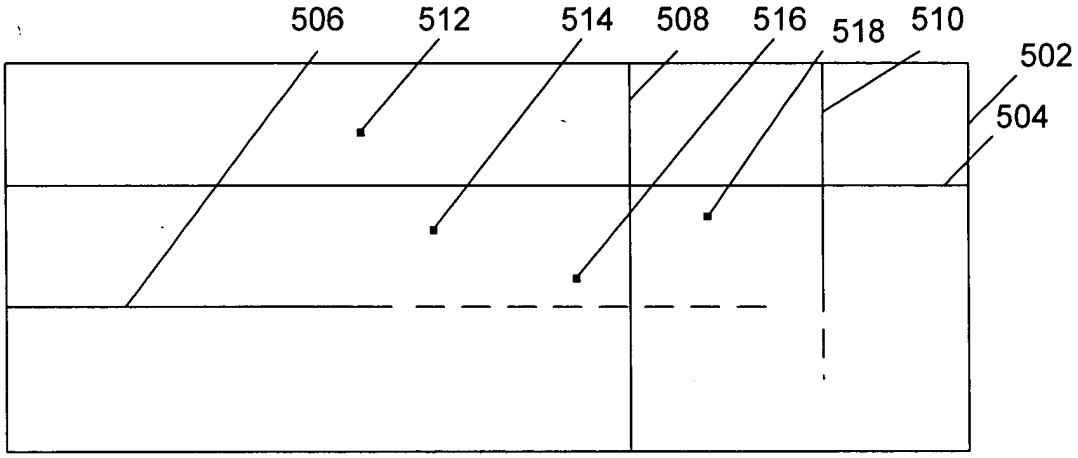

FIG. 5

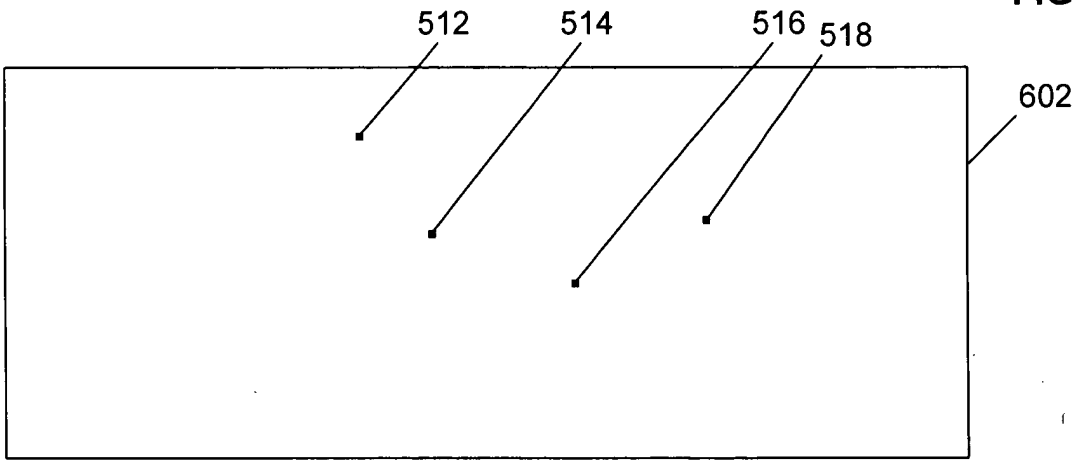

FIG. 6

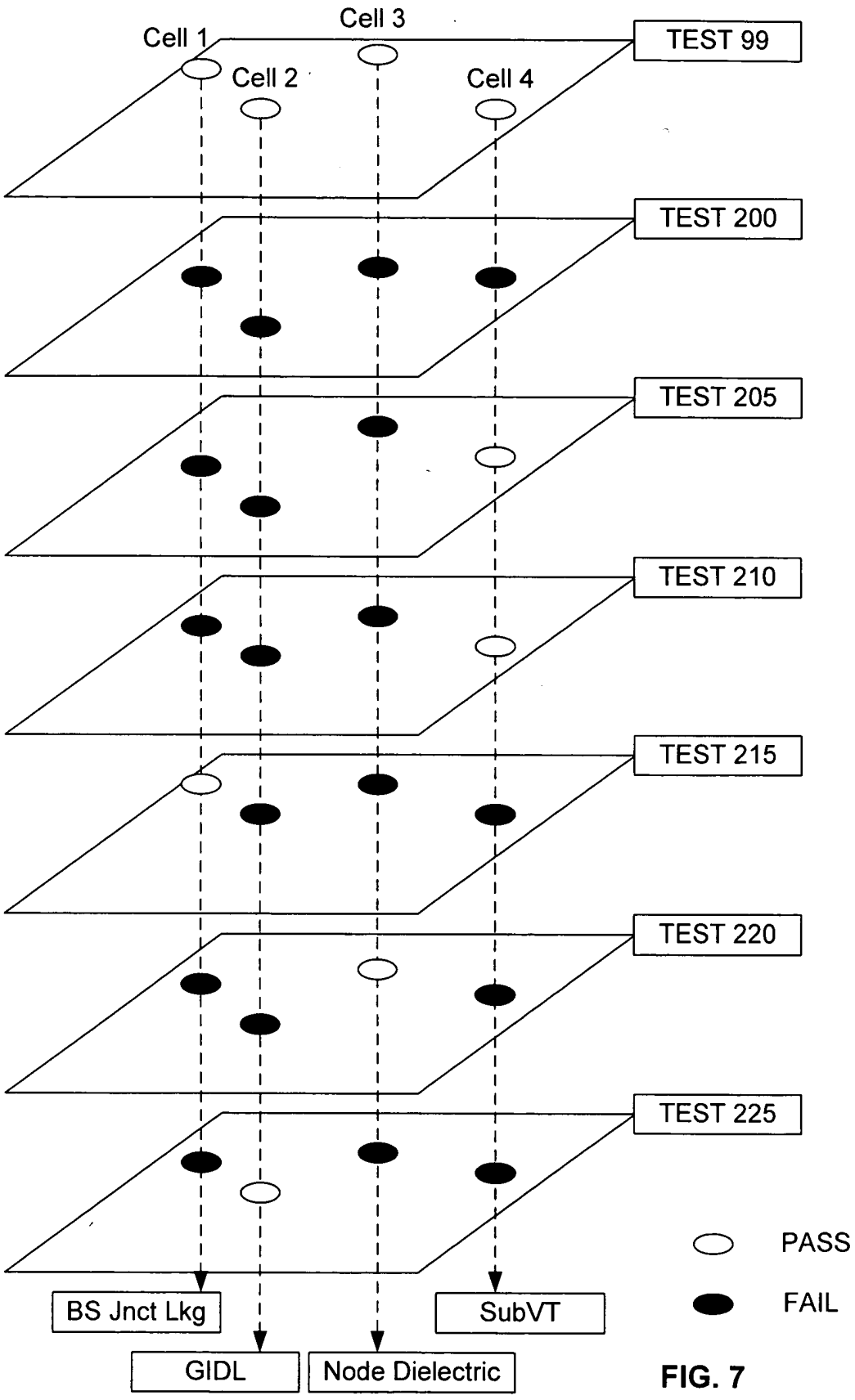
Cell 1
Cell 3
Cell 2
Cell 4
TEST 99
TEST 200
TEST 205
TEST 210
TEST 215
TEST 220
TEST 225
PASS
FAIL
BS Jnct Lkg
SubVT
GIDL
Node Dielectric

FIG. 7

		Test Conditions						identified					
test	Testname	t_{RET} [ms]	bumped?	PWELL V_{BB} [V]	Plate V_{PL} [V]	Bitline Equalize V_{BLEQ} [V]	Bitline High V_{BLH} [V]	BSJ/GIDL	BS Jctn. Lkg.	GIDL	Node Diel.	subVt	vert. FET
99	3VFCN	<<tRET	no	Vbb	Vpl	Vbleq	Vblh	0	0	0	0	0	0
200	SIGA0 (nominal)	tRET	no	Vbb	Vpl	Vbleq	Vblh	1	1	1	1	1	1
205	SIGA1	tRET	yes	Vbb-dVbb	Vpl	Vbleq	Vblh	1	1	1	1	0	0
210	SIGA2	tRET	yes	Vbb+dVbb	Vpl+dVpl	Vbleq+dVbleq	Vblh	1	1	1	1	0	1
215	SIGA3	tRET	yes	Vbb+dVbb	Vpl	Vbleq	Vblh	0	0	1	1	1	1
220	SIGA4	tRET	no	Vbb	Vpl+dVpl	Vbleq	Vblh	1	1	1	0	1	0
225	SIGA5	tRET	yes	Vbb-dVbb	Vpl-dVpl	Vbleq	Vblh	0	1	0	1	1	0
230	SIGA6	tRET	no	Vbb	Vpl-dVpl	Vbleq	Vblh	X	X	X	X	X	X
330	SIGA7 (cum.)	n.a.	yes	n.a.	n.a.	n.a.	n.a.	X	X	X	X	X	X

FIG. 8

		Test Conditions						induced				
test	Testname	t_{RET} [ms]	bumped?	PWELL V_{BB} [V]	Plate V_{PL} [V]	Bitline Equalize V_{BLEQ} [V]	Bitline High V_{BLH} [V]	BS Jctn. Lkg.	GIDL	Node Diel.	subVt	vert. FET
99	3VFCN	<<tRET	no	Vbb	Vpl	Vbleq	Vblh	0	0	0	0	0
200	SIGA0 (nominal)	tRET	no	Vbb	Vpl	Vbleq	Vblh	0	0	0	0	0
205	SIGA1	tRET	yes	Vbb-dVbb	Vpl	Vbleq	Vblh	1	0	0	0	0
210	SIGA2	tRET	yes	Vbb+dVbb	Vpl+dVpl	Vbleq+dVbleq	Vblh	0	1	0	0	0
215	SIGA3	tRET	yes	Vbb+dVbb	Vpl	Vbleq	Vblh	0	0	0	1	1
220	SIGA4	tRET	no	Vbb	Vpl+dVpl	Vbleq	Vblh	0	0	0	0	0
225	SIGA5	tRET	yes	Vbb-dVbb	Vpl-dVpl	Vbleq	Vblh	0	0	0	0	0
230	SIGA6	tRET	no	Vbb	Vpl-dVpl	Vbleq	Vblh	0	0	1	0	1
330	SIGA7 (cum.)	n.a.	yes	n.a.	n.a.	n.a.	n.a.	1	1	1	1	1

FIG. 9

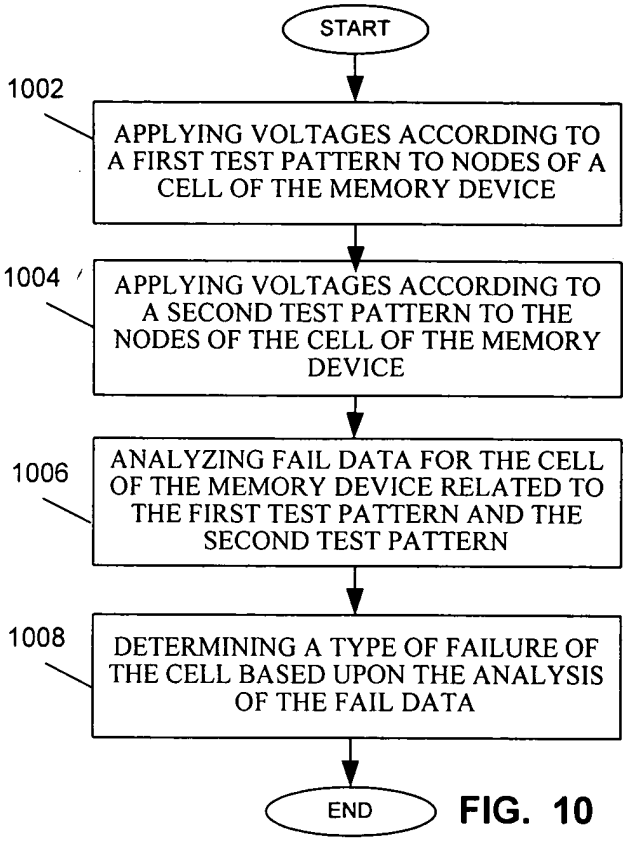

FIG. 10

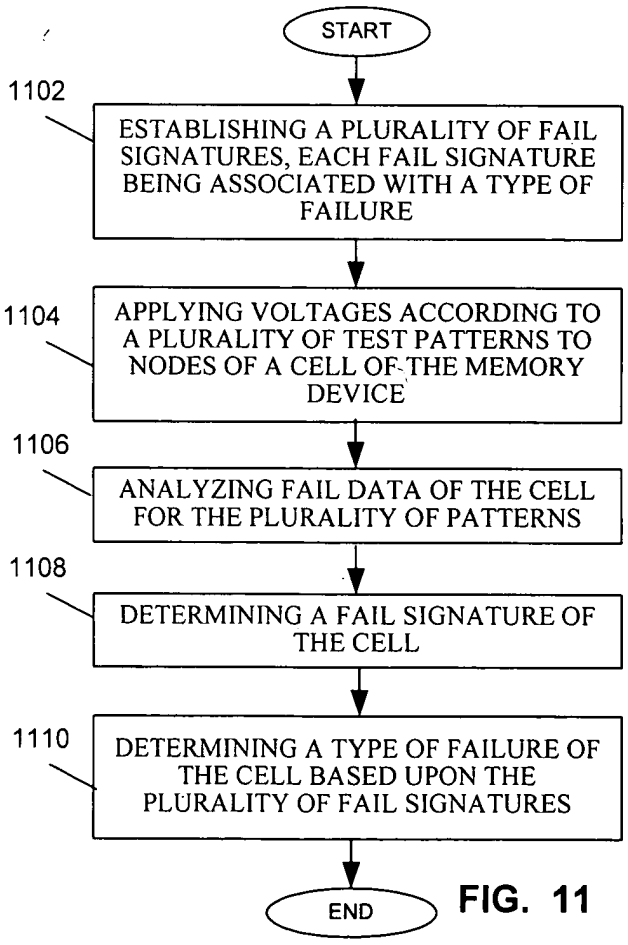

FIG. 11

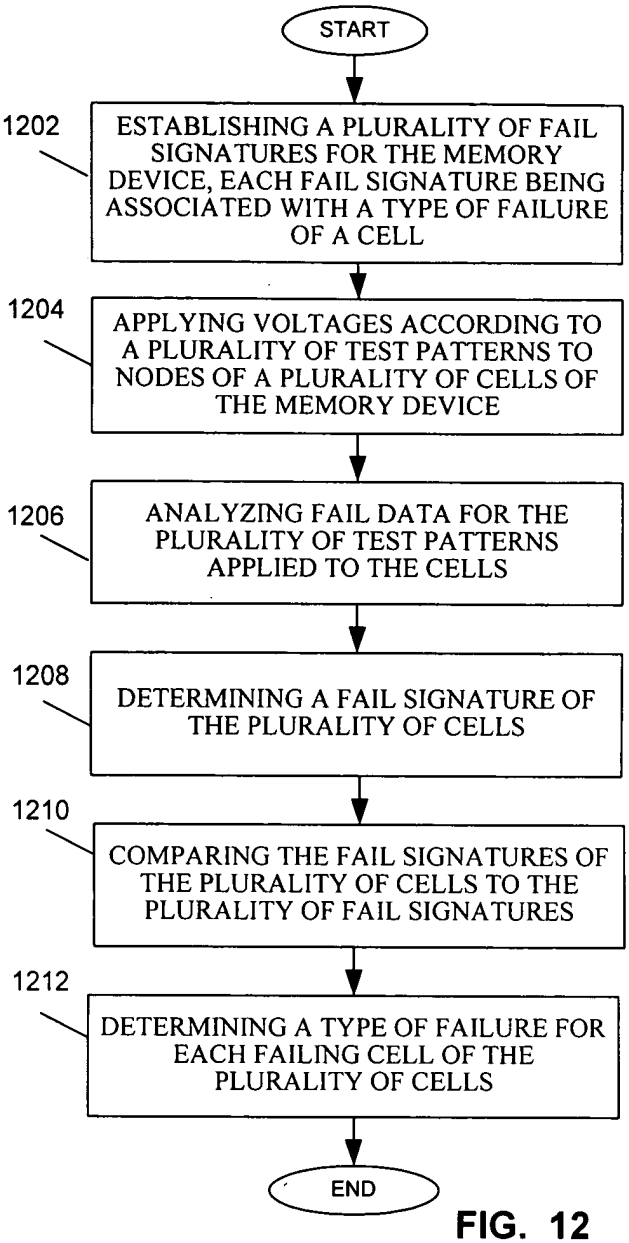

FIG. 12